New approaches are required to feed the ever-increasing need for memory speed.

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High-Speed Source Synchronous Interface Design

As the overall system speed and bandwidth of ASIC interconnects increase, system architects are abandoning traditional interfaces that have become too restrictive. Traditional synchronous interfaces limit interconnect speed to less than 250 MHz and PCB interconnect length to approximately 5 inches. System architects are increasingly turning to source synchronous interconnects that have demonstrated transfer rates of 10^9 transfers per second at distances of 5 meters and more. There are several examples of source synchronous technology within the marketplace, each with a different implementation that affects design complexity and overall performance. Within memory subsystems there are three major examples: DDRSRAM, DDRSDRAM/DDRSGRAM, and RAMBUS DirectRAM. For networking and I/O there are also three examples: SCI, SGI CrayLink, and HIPPI-6400-PH.

A source synchronous interface is one in which data and clock are sent from a transmitter to a receiver, and the clock is used within the receive interface to latch the accompanying data. Source synchronous interfaces have many advantages over traditional synchronous interfaces. Clock frequencies and bandwidth requirements are increasing for emerging systems, CPUs, and chipsets; with synchronous interfaces, time of flight between chips and system-level clock skew are limiting the clock frequencies of buses between chips. Meanwhile, overall pin count of IC-level packaging has not dramatically increased. Source synchronous interfaces remove the limit of the time of flight on wire between two ICs and do not require controlled clock skew between two ICs.

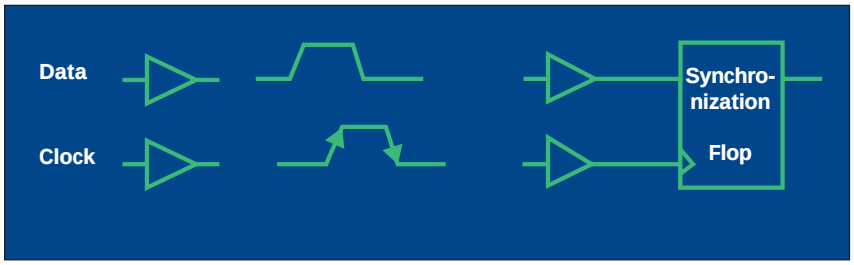


Figure 1. Double data rate interfaces transmit data on both edges of the transmit clock.

Another advantage of source synchronous interfaces is dramatically increased I/O frequencies. Even with increased bandwidth per I/O driver, the number of pins per interface is kept reasonably constant to match the IC packaging technologies available. I/O frequencies can be operated at five to ten times the core logic frequency.

However, source synchronous interfaces create new design challenges. Their interface latency is not necessarily predictable; if predictable latency is required then overall interface latency is increased. Increases in I/O speeds require better electrical performance for IC packages. Because I/O can be operated much faster than core logic, I/O interface logic complexity must be increased to handle the frequency multiplication. Data bit-to-bit timing skews and eye-pattern effects drive overall link operation frequencies; in the past these effects were all but ignored.

Double the Data Rate

A Double Data Rate (DDR) interface (**Figure 1**) outputs data from the transmitter on both edges of the transmit clock (or strobe). This interface offers a way of increasing the bandwidth to memory subsystems (L2/L3 cache, main memory, and frame buffer memory). The trade-off for the increased bandwidth is a more complex interface agent RAM port and more difficult latency prediction due to the asynchronous nature of data reception.

The current standard DDRSDRAM has separate data and address/control interfaces. The data is written and read on both edges of a DQS bidirectional strobe. Address and control are transmitted at one half of the data frequency and latched only on the rising edge of the transmit clock.

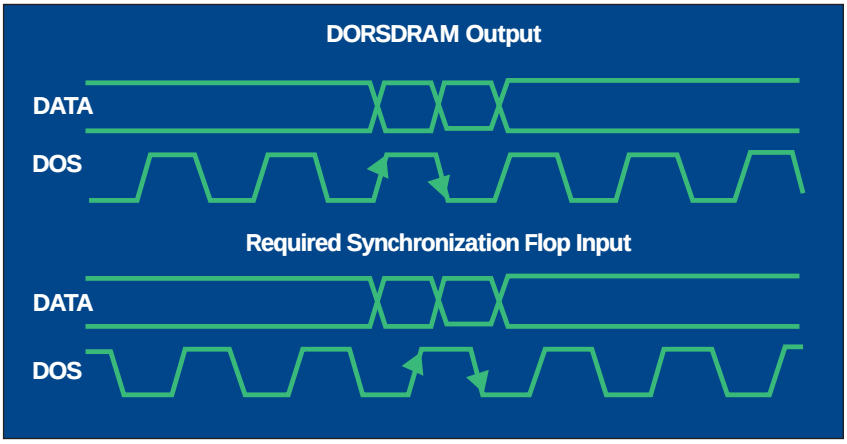


Figure 2. The data and clock are generated synchronously; therefore the clock must be delayed in order to meet the setup and hold time of the reading device.

For the DDRSDRAM interface, data and DQS are driven out of the SDRAM synchronous and in phase (**Figure 2**), requiring setup and hold time at the synchronization flop to be created by delaying DQS. Possible delay techniques are implementation of a PLL/DLL within the interface agent and using a PCB-etch delay line. Either technique will work but will lock the interface into a specific frequency range, reducing flexibility. In addition, the PLL/DLL is IC area intensive for designs that require multiple DDRSDRAMs. Each would place a requirement of two PLLs per RAM on the interface agent IC.

Increased Memory Complexity

There are several factors that increase design and analysis complexity for the DDRSDRAM interface, including interface synchronization, signal quality, and interface timing. Pulse-width distortion and jitter on CLK and DQS cause data and address timing problems at the input to the RAM and interface agent IC's synchronization flop. The jitter component on DQS is further increased by its bidirectional and random nature, unlike the CLK signal which is unidirectional and of constant frequency.

Signal quality is driven by signal line topology, PCB routing and construction, and MIA-package electrical parasitics. For a given signal topology, the overshoot, eye-pattern jitter, and eye-pattern closure can be characterized using a pseudo-random pattern sequence.

Target data rates for DDRSDRAM are 250 Mb/s and greater, requiring clock frequencies of 125 MHz. At these frequencies, poorly terminated or unterminated lines exhibit signal integrity effects that cause settling time to increase. For poorly terminated lines, one factor causing jitter in the settling time is line length approaching tuned resonant length ($^1/_4$ and $^1/_2$ wavelength of the clock frequencies). For a 125-MHz DDRSDRAM the tuned resonant length in FR4 stripline etch for the 250-Mb/s data line is 5.71 inches and 11.43 inches (not accounting for package delays). At these lengths, reflections from the receiver and driver are superimposed on the rising and falling edges of the next data bits, changing the measured settling time of the rising and falling edges. Jitter's effect on settling time also may cause the signal to not settle to a V_{OH} or V_{OL} before the next transition occurs. These effects are commonly referred to as eye-pattern or inter-symbol interference (ISI) effects. As the length and topology of the line grows in complexity, network termination becomes crucial in limiting jitter and its effects.

Line Termination

Proper line termination can be determined based on the operational frequency targets. Because the data bus is bidirectional, it does not lend itself to parallel termination. A more appropriate termination scheme would be series termination within the driver to eliminate components from the PCB. There are upper limits on the effectiveness of series termination within the driver, primarily driven by the tolerance of the series output resistance. Typical process limitations are ±22 percent process variation on discrete resistors. As operational speed increases over 500 Mb/s per I/O, the series resistor tolerance will become a strong factor in eye-pattern jitter and closure.

For DDRSDRAM interface timing there are three main paths to be analyzed: DATA WRITE, DATA READ, and ADDRESS. The goal for these paths is a setup and hold margin that is non-negative after summing all worst-case effects. In some instances where a measurable bit error rate is acceptable

(due to robust error detection and correction), a statistical analysis of the timing may be employed. The DATA signals have the most difficult timing to analyze due to their high speed and dual-edge latching. ADDRESS timing can also be difficult due to the multi-load bus, but this is typically solved through good driver design and proper topology construction.

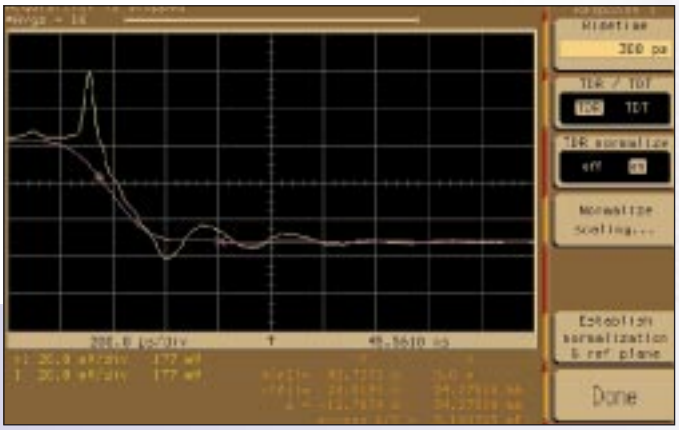
Each timing path can be divided into three sections: transmit timing, interconnect timing, and receive timing. Transmit timing includes all possible components of timing jitter and skews within the transmitting IC that would subtract from either setup or hold at the synchronizing latch within the receiving IC. For DATA WRITE and ADDRESS, the transmit section is the interface agent output drive. The interface agent needs to reduce the overall skew and jitter between the data bits and the strobe (DQS) to an overall minimum. The skew components come from clk-q and t_{pd} delay differences in the flops, boundary-scan components, and output driver. Jitter can come from PLL or oscillator jitter, AC fluctuations on the power supplies due to core switching events, and output switching events.

Include Jitter and Skew in Timing Estimates

Interconnect timing includes all jitter and skew components that subtract from the setup and hold at the receiving-IC flop. For all paths, the interconnect timing components are due to trace length and dielectric constant differences between data lines in the PCB and package.

Receive timing is all the jitter and skew components that subtract from the synchronizing flop's setup and hold margin. Receive timing for DATA WRITE and ADDRESS is defined by the DDRSDRAM vendor. For DATA READ receive timing, the interface agent needs to reduce the skew and jitter between the data bits and DQS to an overall minimum in the receive block. The skew components come from t_{pd} delay differences in the boundary scan components, input receiver, and strobe routing.

These three paths were analyzed under three sigma conditions for silicon process, PCB process, voltage, and temperature. A study shows that a DDRSDRAM interface can be easily implemented with no less than 7 percent of performance margin for all timing paths. As DDRSDRAM vendors improve input and output timing specifications, the analysis shows that performance for this interface will rapidly approach 500 Mb/s.



Remove Effects of the Test Fixture

High-speed memory buses can operate only if the circuit-board traces function in a controlled impedance environment. For example, the Direct RAMBUS requires an impedance of 28 Ω which must be maintained to within ±2.8 Ω. When making measurements to ensure that the proper environment is maintained, you will find that the test fixture always affects the measurement in some way.

An enhancement of standard TDR waveforms is needed to ensure compliance with the impedance requirements. The normalization function of the HP 54750A Digitizing Oscilloscope corrects for the test fixture errors. The measured response is first converted to the frequency domain. Once in this domain, the Digitizing Oscilloscope filters the data based on a reference plane from data taken during a 50Ω and short-circuit calibration procedure. The filtered data is then converted back into the time domain and displayed without the artifacts created by the test fixture.

As shown above, the measured response of a 28-Ω microstrip shows a knee that is not characteristic of the DUT. The superimposed waveform is normalized, yielding an impedance measurement with enhanced accuracy.

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